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(54) INITIALIZATION METHOD FOR DATA SWITCHING SYSTEM

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Claim

An initialization method for a data switching system, characterized by the fact that in an initialization method for data service units of a data switching system constituted by connecting data devices having several transmission and reception channels to a data switching exchange via an above-mentioned data service unit for each channel, the transmission timing of a channel reset request signal transmitted from each said data service unit to data said data switching exchange is made different from that of the other respective data service units at the time of initialization.

Detailed explanation of the invention

Technical field

The present invention pertains to a data switching system in which data devices or data terminals are connected to a data switching exchange via data service units for each transmission and reception channel. In particular, the present invention pertains to an improvement of a method for collectively initializing the above-mentioned respective data service units.

Technical background of the invention

A recent example of a data switching system is one in which data devices 2, consisting of large-scale computers (host CPU) or data terminals (TSS) 3 such as facsimile devices, are

connected to a data switching exchange 1 via data service units (DSU) 41-4n for each transmission and reception channel, and data are transmitted between desired channels while controlling the communication for each transmission and reception channel by means of the above-mentioned data service units 41-4n as shown in Figure 3. In the figure, 51-5n are communication lines, and 61-6n are terminal lines.

Figure 4 shows the constitution of the above-mentioned data service units 41-4n, where each data service unit consists of central control part (CPU) 7a, memory 7b for storing operation programs for the CPU 7a, communication control part 7c for controlling communication in a prescribed sequence according to control of the above-mentioned CPU 7a, and initial circuit 7d for operation at the time of initialization. In addition, these data service units 41-4n are arranged in blocks for each data device 2, and power from a power supply circuit 8 is received by the units of the block 4.

Now in such a conventional switching system, if power of the power supply circuit 8 is input when the system is started or restarted after overcoming obstacles, the system operates as follows. In other words, if the power of the power supply circuit 8 is input, its power supply output is supplied to each data service unit 41-4n via a power supply line 8a. As a result, each initial circuit 7d is operated to reset the CPU 7a. Each CPU 7a then implements an initial program stored in each memory 7b to initialize each part in the unit, and transmits a switching exchange channel reset request signal to the data switching exchange 1 to report the initialization. When the arrival of the above-mentioned reset request signal is detected, the data switching exchange 1 in response implements processing related to the channel reset request signal from each above-mentioned data service unit 41-4n prior to other processing to be implemented, for example, processing related to a connection request from another data device 2 or data terminal 3. After processing for all the channel reset request signals is finished, processing for the connection request from the above-mentioned other data device or data terminal is implemented.

Problems of the prior art

In the conventional initialization method, however, since the respective data service units 41-4n were simultaneously initialized and transmitted channel reset request signals to the data switching exchange 1 when power was input, channel reset request signals corresponding in number to the number of said data service units were simultaneously concentrated at the data switching exchange 1, so that the data switching exchange 1 was fully involved in the processing of each said channel reset request signal, and could not implement other processing for connection requests, etc. This [other] processing was thereby greatly delayed.

Objective of the invention

The objective of the present invention is to provide an initialization method for a data switching system in which the load concentration at a data switching exchange is prevented by preventing channel reset request signals sent to the data switching exchange from data service units from being generated simultaneously, so that there are no negative effects on other processing.

Outline of the invention

In order to achieve the above-mentioned objective according to the present invention, at the time of an initialization operation, the transmission timing of channel reset request signals from the respective data service units to a data switching exchange is made different so that load concentration at the data switching exchange is prevented.

Application example of the invention

Figure 1 shows the constitution of data service units to which the initialization method in an application example of the present invention is applied. Here, the same symbols will be given to the same parts in the figure as those of the above-mentioned Figure 4, and their detailed explanation will be omitted. In addition, since each data service unit 401-40n has the same constitution, only the constitution of the unit 401 is explained.

The data service unit 401 is equipped with a counter 9a1 and a comparator 9b1 as an initial circuit, in addition to a control circuit 71 comprising the CPU 7a, memory 7b, and communication control part 7c shown in the above-mentioned Figure 4. The counter 9a1 is operated by a common reset circuit 9 provided for all the data service units 401-40n, starts counting a clock signal CK generated by the reset circuit 9 from the moment that a reset signal RS is generated by said reset circuit 9, and outputs the count value to the comparator 9b1. The comparator 9b1 continuously compares the count value output from the above-mentioned counter 9a1 with a separately set reference value T1, and generates an initializing signal IR1 to make the control circuit 71 implement an initialization operation when the count value reaches the reference value T1. Here, the reference value T that is set in the above-mentioned comparator is made different for the respective data service units 401-40n, and the values are set so that the value T for data service unit 401 is the smallest, and the value increases toward unit 40n.

With this constitution, if power is input to a power supply circuit 8, the power output PW is supplied to each data service unit 401-40n and to the reset circuit 9. As shown in Figure 2, for instance, the reset signal RS is thus generated by the reset circuit 9 at time t0 when the above-mentioned power output PW is supplied, so that the respective counters 9a1-9an in each data service unit 401-40n start counting the clock signal CK simultaneously. Then, when the count

value equals the reference value T1-Tn, initializing signals IR1-IRn are respectively generated from each comparator 9b1-9bn, as shown in Figure 2. As a result, the control circuits 71-7n respectively start an initializing operation when the above-mentioned initializing signals IR1-IRn are generated, and each control circuit transmits a channel reset request signal to a data switching exchange 1 from the communication control part 7c after finishing its own initialization. The transmission timing of each channel reset signal from the respective data service units 404-40n to the data switching exchange 1 is shifted relative to the others.

As described above, in this application example the counters 9a and the comparators 9b are installed in the initial circuits, and the initialization start timing for each data service unit 401-40n is shifted relative to the others, so that the timing of the channel reset request signals transmitted from each data service unit 401-40n to the data switching exchange 1 can be made different. A concentration of channel reset request signals on the data switching exchange 1 can thereby be prevented. As a result, even if separate processing requests such as connection requests from data terminals are generated in a processing period corresponding to that of the above-mentioned channel reset request signals, the processing corresponding to the processing requests can be implemented during processing of the channel reset request signals from each data service unit 401-40n, so that the delay of other processing can be greatly reduced. In addition, since the constitutions of all the respective data service units 401-40n are made the same, and only the reference values T1-Tn that are supplied to each comparator 9b1-9bn are made different from each other; for example, the constitution of the data service units can be markedly simplified, compared with the case in which the initialization timing is made different by changing the initial program for each data service unit.

Moreover, the present invention is not limited to the above-mentioned application example. For example, in the above-mentioned application example, the timing of the initialization operation itself of each data service unit 401-40n has been made different from the others. However, the initializing operation itself may be simultaneously carried out, and only the transmission timing of the channel reset request signals can be made different. Furthermore, delay circuits can be respectively installed in each data service unit 401-40n, and the amount of delay is shifted for each, so that the transmission timing of the channel reset request signals can be made different. In addition, the constitution of the initialization means, the transmission sequence of the channel reset request signals, and the timing can be variously modified within a range that does not depart from the gist of the present invention.

Effect of the invention

As described above in detail, according to the present invention, at the time of an initializing operation, the timing of channel reset request signals transmitted from each data

service unit to the data switching exchange is made different for the respective data service units, so that the channel reset request signals transmitted to the data switching exchange from the data service units are not generated simultaneously, thereby preventing a load concentration at the data switching exchange. As a result, an initialization method for a data switching system can be provided that prevents negative effects on other processing.

Brief description of the figures

Figures 1 and 2 help explain the initialization method in an application example of the present invention. Figure 1 is a circuit block diagram showing the constitution of data service units to which said method is applied, and Figure 2 is a timing chart illustrating the operation of said units. Figures 3 and 4 help explain a conventional initialization method. Figure 3 shows an example of the constitution of a data switching system, and Figure 4 is a circuit block diagram showing the constitution of the data service units.

1	Data switching exchange
2	Data device
3	Data terminal
8	Power supply circuit
9	Reset circuit
9a1-9an	Counters
9b1-9bn	Comparators
40	Data service unit block
404-40n	Data service units
51-5n	Communication lines
61-6n	Terminal lines
71-7n	Control circuits
CK	Clock signal
IR1-IRn	Initializing signals
RS	Reset signal

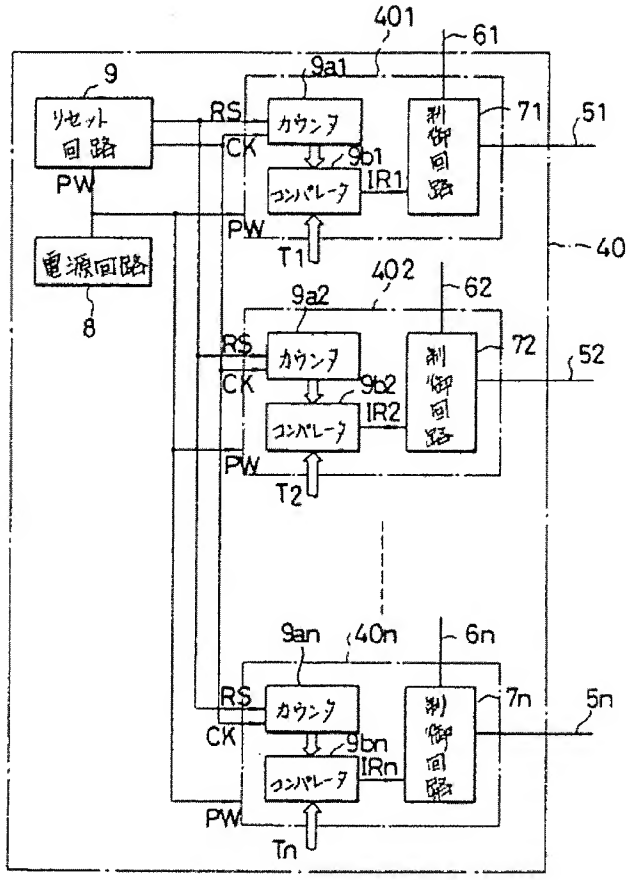

Figure 1

Key:

8	Power supply circuit
7n	Control circuit
9	Reset circuit
9a1	Counter
9b1	Comparator
9a2	Counter
9b2	Comparator
9an	Counter
9bn	Comparator
71	Control circuit
72	Control circuit

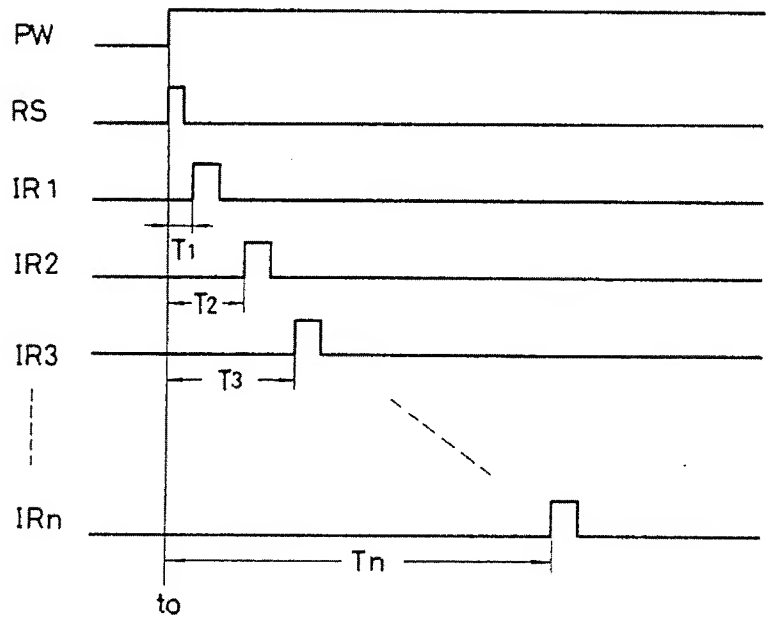

Figure 2

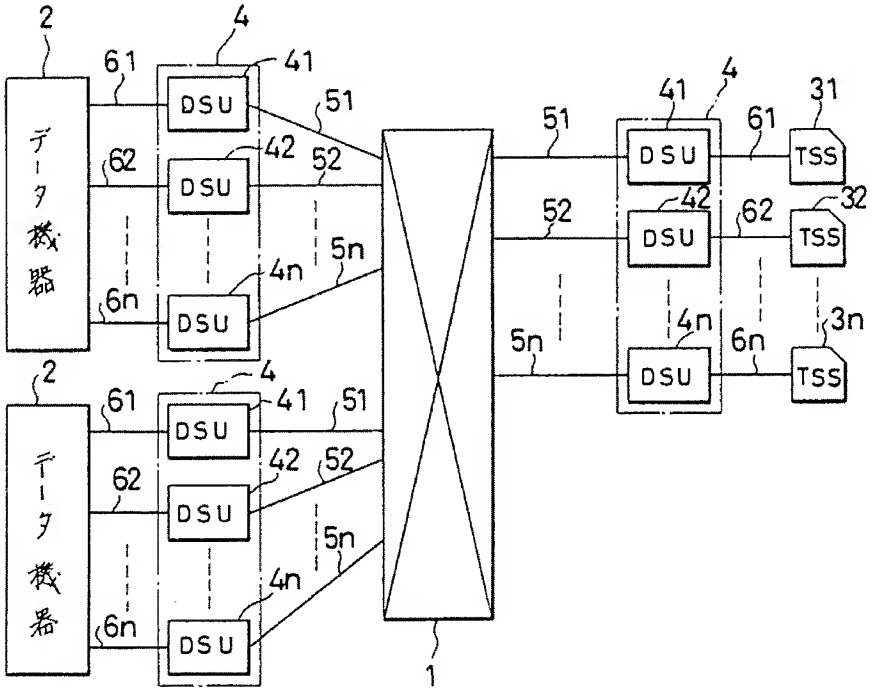

Figure 3

Key: 2 Data device

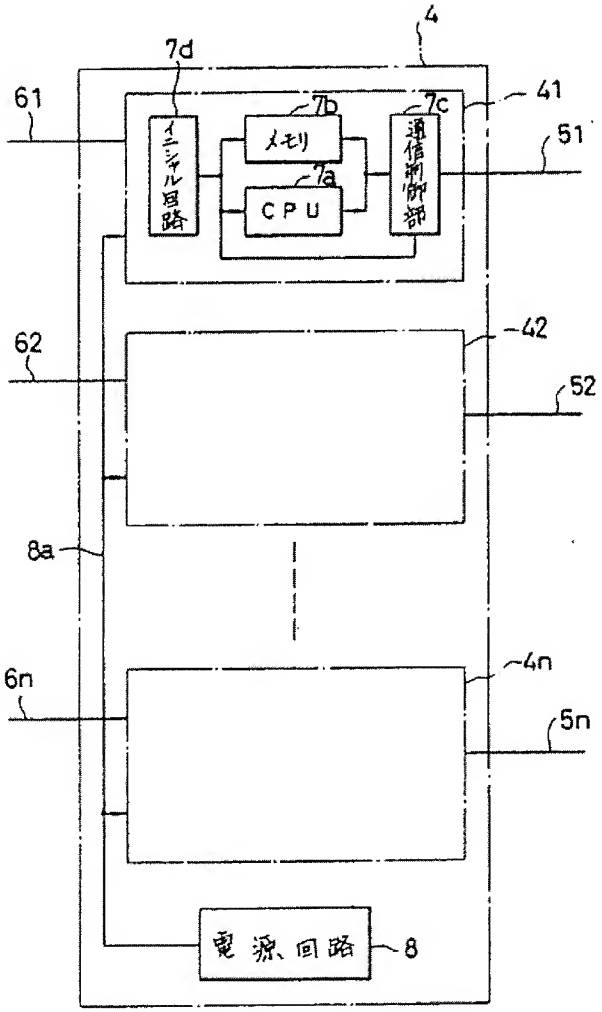

Figure 4

Key:
- 7b Memory
- 7c Communication control part
- 7d Initial circuit
- 8 Power supply circuit